AM4534C

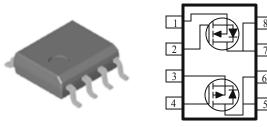
Analog Power

P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low r_{DS(on)} Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUC	PRODUCT SUMMARY			
V _{DS} (V)	$r_{DS(on)} m(\Omega)$	I _D (A)		
30	$40 @ V_{GS} = 4.5V$	6.0		
50	$28 @ V_{GS} = 10V$	7.0		
-26.5	$80 @ V_{GS} = -2.5V$	-4.0		
-20.3	$52 @ V_{GS} = -4.5V$	-5.2		



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)							
Parameter		Symbol	N-Channel	P-Channel	Units		
Drain-Source Voltage		V _{DS}	30	-26.5	v		
Gate-Source Voltage		V _{GS}	±20	±12			
	$T_A=25^{\circ}C$	I _D	7	-5.2	А		
Continuous Drain Current ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$		5.6	-6.8			
Pulsed Drain Current ^b		I _{DM}	20	-20			
Continuous Source Current (Diode Conduction) ^a		Is	1.3	-1.3	А		
	$T_A=25^{\circ}C$	-P _D	2.1	2.1	W		
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$		1.3	1.3			
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
Maximum Junction-to-Case ^a	t <= 5 sec	$R_{\theta JC}$	40	°C/W		
Maximum Junction-to-Ambient ^a	t <= 5 sec	$R_{\theta JA}$	60	°C/W		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

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	Symbol	LESS OTHERWISE NO	Limits				
Parameter			Ch	Min	Тур	Max	Unit
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 V, I_D = 250 uA$	Ν	30			v
	V (BR)DSS	VGS = 0 V, ID = -250 uA	Р	-26			
Gate-Threshold Voltage	V _{GS(th)}	VGS = VDS, $ID = 250 uA$	N	1			v
Gate-Inconoid Voltage	· 03(iii)	$V_{GS} = V_{DS}$, $I_D = -250 \text{ uA}$	Р	-1		100	Ľ
Gate-Body Leakage Zero Gate Voltage Drain Current	I _{GSS}	$V_{GS} = -12 V, V_{DS} = 0 V$	P N			$\pm 100 \\ \pm 100$	nA
	+ +	$\frac{V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}}{V_{DS} = -21.2 \text{ V}, V_{GS} = 0 \text{ V}}$	P			±100 -1	
	I _{DSS}	$V_{DS} = 24 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	N			1	uA
On-State Drain Current ^A	Т	$V_{DS} = 5 V, V_{GS} = 10 V$	Ν	20			А
	I _{D(on)}	$V_{DS} = -5 V, V_{GS} = -4.5 V$	Р	-20			A
		VGS = 10 V, ID = 7 A	N			28	
Drain-Source On-Resistance ^A	r _{DS(on)}	VGS = 4.5 V, ID = 6 A	11			40	mΩ
Brain Source on Resistance		VGS = -4.5 V, ID = -5 A	Р			52 80	
		VGS = -2.5 V, ID = -4 A $V_{DS} = 15 V, I_D = 7 A$	N		25	80	<u> </u>
Forward Tranconductance ^A	$g_{\rm fs}$	$V_{DS} = -15 \text{ V}, \text{ I}_D = -5 \text{ A}$	N P		10		S
Dynamic		· ·					
Total Gate Charge	Qg	N-Channel V _{DS} =15V, V _{GS} =10V, I _D =7A	Ν		4		nC
Total Gate Charge	√g		Р		25		
Gate-Source Charge	Q _{gs}		N		1.1		
	1 50	P-Channel	P N		2.4		ne
Gate-Drain Charge	Q_{gd}	VDS=-15V, VGS=-4.5V, ID=-5A		+			
Switching	<u> </u>		Р		3.9		
8			N	г	8		
Turn-On Delay Time	t _{d(on)}	N-Chaneel $V_{\text{DD}}{=}15V, V\text{GS}{=}10V, \text{ID}{=}1A \ , \\ R_{\text{GEN}}{=}6\Omega, \label{eq:generalized}$	P		7		
Rise Time	t _r		N		5		nS
	.1		Р		13		
Turn-Off Delay Time	$t_{d(off)}$	P-Channel VDD=-15V, VGS=-4.5V, ID=-1A	N P	┥	23 14	1	
Fall Time	+	RGEN= 6Ω	N		3		
Fall-Time	t _f		Р		9	1	Í

Notes

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- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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